REMARKS

In the Office Action, the Examiner allowed claims 2, 4, 6, 11-18, 21, 23 and 32-40 and objected to claims 3, 5, 20, 22, 28 and 46 as being dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1, 7-10, 19, 24-27, 29-31, 41-45 and 47 are rejected. Claims 1-47 are pending.

The Examiner rejected claims 1, 7, 9, 10, 27, 29-30, and 45 under 35 U.S.C. § 102(b) as being unpatentable under U.S. Patent No. 5,608,816 (***Kawahara***). Applicants respectfully traverse this rejection.

The Examiner misapplied ***Kawahara*** to read upon the elements of claims 1 and 45 of the present invention. ***Kawahara*** is merely directed to the examination of a printed wiring board. ***Kawahara*** is generally referring to a printed circuit (PC) board. The Examiner mistakenly uses subject matter related to a printed wiring board to assert an anticipation rejection of claims directed to a method and apparatus of analyzing a wafer. Applicants respectfully assert that the anticipation rejection based upon a printed wiring board being used reject claims relating to analyzing a wafer is inappropriate. ***Kawahara*** simply does not disclose analyzing patterns on a wafer. The Examiner cited the printed wiring board 13 to read upon the wafer called for by claims 1 and 45 of the present invention. Applicants respectfully assert that the printed wiring board 13 is not a wafer, and that the Examiner erred in making such as assertion. Therefore, the Examiner use of ***Kawahara*** to reject claims 1 and 45 under 35 U.S.C. § 102(b) using ***Kawahara*** is flawed. Furthermore, *arguendo*, even if an anticipation rejection under ***Kawahara*** were appropriate, ***Kawahara*** simply does not disclose all of the elements of claim 1 and 45.

Kawahara does not disclose determining a dimension of a grid on a test structure on a wafer by measuring light reflected from an illuminated portion of the grid, as called for by claim 1 of the present invention. ***Kawahara*** discloses that a reflecting lighting 18 is used to illuminate the printed wiring board 13with diffused light from above and transmitted lighting 19 for illuminating the board 13 with a pulsed from under board 13. *See*, col. 12, lines 42-46. ***Kawahara*** also discloses that a grey level image of the holed wiring pattern and through-hole illuminated by the reflecting and transmitting lights 18, 19 is produced. *See*, col. 12, lines 46-52. However, ***Kawahara*** does not disclose illuminating a grid with at light source and measuring the light reflected from the illuminated portion of the grid on a wafer, as called for by claim 1 of the present invention. Further, ***Kawahara*** does not disclose determining a dimension of the grid based upon the reflection profile. In fact, ***Kawahara*** does not even disclose a grid. Additionally, the Examiner admitted that ***Kawahara*** does not disclose provide detail of the pattern, wherein claims 1 calls for analyzing a grid. *See*, page 2 of the Office Action dated June, 29, 2005. The Examiner merely asserts that the pattern is an inherent feature of a wiring pattern. *Id.* The Examiner does not provide evidence in the prior art or arguments to support this contention.

Further ***Kawahara*** does not disclose a reflection profile. ***Kawahara*** merely measure discloses determining a gray level image of the holed wiring pattern and the through-hole. There is simply no mention of the reflection profile called for by claim 1, in ***Kawahara***. Additionally, ***Kawahara*** does not disclose examining a grid; much less determining a dimension of the grid based upon the reflection profile, as called for by claim 1 of the present invention. Accordingly, even if, arguendo, the printed wiring board is used to anticipate the wafer, various other elements of claim 1 of the present invention are not taught, disclosed, or suggested by ***Kawahara***.

Kawahara simply discloses design rule checks to measure width of the wiring pattern and specifics shapes, such as corners, on a printed wiring board. *See*, col. 18, lines 55-68. ***Kawahara*** does not disclose measuring the dimensions of a grid, as called for by claim 1 of the present invention. ***Kawahara*** is directed to measuring pattern widths of a wiring patter, shapes of branching points to detect defective wiring pattern, *e.g.*, shortage of wiring patter, electric short or open. *See*, col. 19, lines 49-59. ***Kawahara*** clearly does not disclose determining a dimension of a grid on a wafer based upon reflection profile. Therefore, as mentioned above, there are several reasons why ***Kawahara*** does not teach, disclose, or suggest all of the elements of claim 1 of the present invention. Hence, claim 1 is allowable for at least the reasons cited above.

Additionally, claim 27 calls for a metrology tool comprising a data processing unit for determining a dimension of the grid based upon a reflection profile, which are elements not taught or suggested by ***Kawahara***. Therefore, claim 24 is also allowable for at least the reasons cited above. Additionally, claim 45 calls for a metrology tool comprising means for determining a dimension of the grid based upon a reflection profile, which are elements not taught or suggested by ***Kawahara***. Therefore, claim 45 is also allowable for at least the reasons cited above.

Independent claim 1, 27, and 45 are allowable for at least the reasons cited above. Further, dependent claims, claims 2-10, 28-31, and 46-47, which depend from 1, 27, and 45, respectively, are allowable for at least the reasons cited herein.

The Examiner rejected claim 42 under 35 U.S.C. § 102(e) as being unpatentable under U.S. Patent No. 6,594,598 (***Ishizuka***). Applicants respectfully traverse this rejection.

The Examiner cited Figure 3(a) to assert anticipation of the test structure comprising a first plurality of line and a second plurality of lines intersecting the first plurality of lines to define a grid, as called for by claim 42. However, Applicants respectfully assert that the disclosure of Figures 3(a)-3(c) of ***Ishizuka*** merely refer to a graph and a wafer that contains a plurality of semiconductor chips. *See*, col. 8, line 66-col. 9, line 5. The Examiner misconstrued the semiconductor chips in the wafers illustrated of Figure 3(a)-3(c) to mean the grid called for by claim 42. Figures 3(a)-3(c) refer to semiconductor chips and not grid on a test structure. Therefore, all of the elements of claim 42 is not anticipated or suggested by ***Ishizuka***. Accordingly, claim 42 of the present is allowable for at least the reasons cited above.

The Examiner rejected claims 8, 19, 24-26, 31, 41, and 47 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,608,816 (***Kawahara***). Applicants respectfully traverse this rejection.

Regarding claims 8, 31, and 47, the Examiner asserted that it would have been obvious to provide a comparison to ensure proper sizing for proper component placing. The Examiner fails to provide any evidence or arguments to support this assertion. The Examiner does not point to any disclosure in ***Kawahara*** or other prior art evidence to assert obviousness of the comparison to ensure proper sizing for proper component placing. Further, Applicants respectfully assert that ***Kawahara*** does not teach or make obvious other elements of claims 8, 31, and 47 as described above. For example, ***Kawahara*** does not disclose or make obvious method or apparatus relating to determining a dimension of a grid on wafer based upon a reflection profile (as described above). Therefore, adding the unproven and unsupported assertion regarding the comparison to ensure proper sizing for proper component placing would still not render all of the elements of claims 8, 31, and 47 obvious or anticipated. Further, ***Kawahara*** is not analogous art

since it is directed to printed wiring boards and the claims relate to wafers. Those skilled in the art would not use the disclosure of ***Kawahara*** to modify its subject matter and make obvious all of the elements of claims 2, 31, 47. For at least these reasons, claims 8, 31, and 47 are allowable.

Furthermore, all of the elements of claims 19 and 41 and are not made obvious by ***Kawahara***. ***Kawahara*** does not disclose or make obvious method or apparatus relating to determining a dimension of a grid on wafer based upon a reflection profile (as described above). Adding the unproven and unsupported assertion regarding the comparison to ensure proper sizing for proper component placing would still not render all of the elements of claims 19 and 41 obvious or anticipated for at least the reasons cited above. The Examiner does not provide evidence or arguments to the contrary. Further, ***Kawahara*** is not analogous art since it is directed to printed wiring boards and the claims relate to wafers. Those skilled in the art would not use the disclosure of ***Kawahara*** to modify its subject matter and make obvious all of the elements of claims 19 and 41. For at least these reasons, claims 19 and 41 are allowable.

Regarding claims 24, 25, and 26, for at least the reasons described above, several elements of claim 23, from which claims 24, 25, and 26 depend, are not disclosed or made obvious. For example ***Kawahara*** does not disclose or make obvious determining a dimension of a grid on a wafer based upon a reflection profile. Merely adding the concepts of intensity of reflected light, fault condition, and/or width dimension does not anticipate or make obvious all of the elements of claim 24, 25, and 26. ***Kawahara*** simply does not disclose or make obvious determining a dimension of a grid on a wafer based upon a reflection profile. Further, ***Kawahara*** is not analogous art since it is directed to printed wiring boards and the claims relate to wafers. Those skilled in the art would not use the disclosure of ***Kawahara*** to modify its subject matter

and make obvious all of the elements of claims 19 and 41. For at least these reasons, claims 24, 25, and 26 are allowable.

The Examiner rejected claims 43-44 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,594,598 (***Ishizuka***) in view of U.S. Patent No. 5,608,816 (***Kawahara***).

As described above, ***Ishizuka*** does not disclose or make obvious the test structure and the first and second plurality of lines that form the grid, as called for claim 42, from which claims 43 and 44 depend. The disclosure of ***Kawahara*** does not make up for this deficit. Further, without improper hindsight reasoning, those skilled in the art would not combine the disclosure of ***Kawahara***, which is directed to a printed wiring board, with ***Ishizuka***, which is directed to semiconductor wafer. There is no evidence that those skilled in the art would combine the printed wiring disclosure of ***Kawahara*** with the wafer disclosure of ***Ishizuka***. Additionally, as described above even if ***Ishizuka*** and ***Kawahara*** were to be combined, all of the elements would still not be taught or make obvious by ***Ishizuka***, ***Kawahara*** or their combination. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness by failing to show the requisite teaching or suggestion to combine the prior references. Therefore, claims 43-44 are allowable for at least the reasons cited herein.

Applicants acknowledge and appreciate that claims 2, 4, 6, 11-18, 21, 23 and 32-40 have been allowed. Additionally, acknowledge and appreciate that the Examiner has asserted that claims 3, 5, 20, 22, 28 and 46 contain allowable subject matter. Further, Applicants respectfully assert that all claims of the present invention are allowable.

Reconsideration of the present application is respectfully requested.

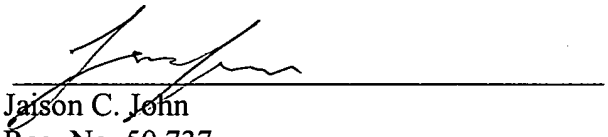
In light of the arguments presented above, Applicants respectfully assert that claims 1-47 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

In view of the remarks set forth herein, the application is believed to be in condition for allowance and notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the **Examiner is requested to contact the undersigned attorney at (713) 934-4069** with any questions, comments or suggestions relating to the referenced patent application.

WILLIAMS, MORGAN & AMERSON

CUSTOMER NUMBER 23720

Respectfully submitted,



Jaison C. John
Reg. No. 50,737

Attorney for Applicants

10333 Richmond Dr., Suite 1100
Houston, Texas 77042
(713) 934-7000

Date: September 29, 2005